YIELD PREDICTION AS A FACTOR IN PRODUCTIVITY MANAGEMENT OF SEMICONDUCTOR PROCESS

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The cycle time to manufacture parts for the semiconductor industry strongly hinders the high productivity of most companies. At times, to be able to contend with the lengthy production cycle time, companies make unnecessary capital expenditures and inventory allocation, which could affect the asset utilization during slow times. This paper discusses the effects and the impact of yield prediction on the productivity and efficiency of semiconductor manufacturing processes. As with other industries, the semiconductor industry goes through cycles (Lara Chamness, 2012). During critical economic situations, companies that have good yield prediction systems in place have more chances of getting through the crisis with only minor dips in its bottom line (Wu, Erkoc, & Karabuk, 2005). Yield prediction is applicable to various types of semiconductor products, whether commodities or high-margin parts. The use of yield prediction models will also have managerial implications on the areas of operations planning, marketing, and finance.

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I. INTRODUCTION AND OVERVIEW OF THE SEMICONDUCTOR INDUSTRY

The semiconductor industry, just like any other industry, experiences boom-bust cycles every so often. The last two decades proved to be tumultuous for the whole semiconductor industry, as evidenced by the cyclical trends. The industry experienced tremendous growth with the burgeoning of the Internet in the early 90's as shown in Fig. 1 (Global Semiconductor Market Forecast to 2015, 2012) (Gross & Hester, 2002). Although the industry still went through the normal cyclical behavior of the market, the trend of the worldwide revenues is going up, and this up-trend growth continued until the mid-2000's. The industry experienced huge cyclical dips and during slow years, decline in revenues accelerated so fast and this caught most the industry players unprepared for the sudden drop in market demand.

For instance, in 2009, when production volumes and capacity utilization of semiconductor plants plunged drastically, shown in Fig. 2 (SICAS Annual Capacity Report, 2010), several companies did not survive and had to close down, or sell out to competitors and other bigger companies. Most companies braced for the worst, revenues and volumes slid down and earnings dipped down to the negatives. Even industry giants were not spared.

The huge market expansion for the semiconductor industry during the last decade was mainly propelled by the market's appetite for mobile devices and telecommunications paraphernalia. The world suddenly shrunk in size and it became easier to reach anybody even from across continents. Smartphones, tablets and ultraportable devices became a necessity for most consumers due to their insatiable need to be able

FIGURE 1: GLOBAL SEMICONDUCTOR REVENUES (1976 – 2011)

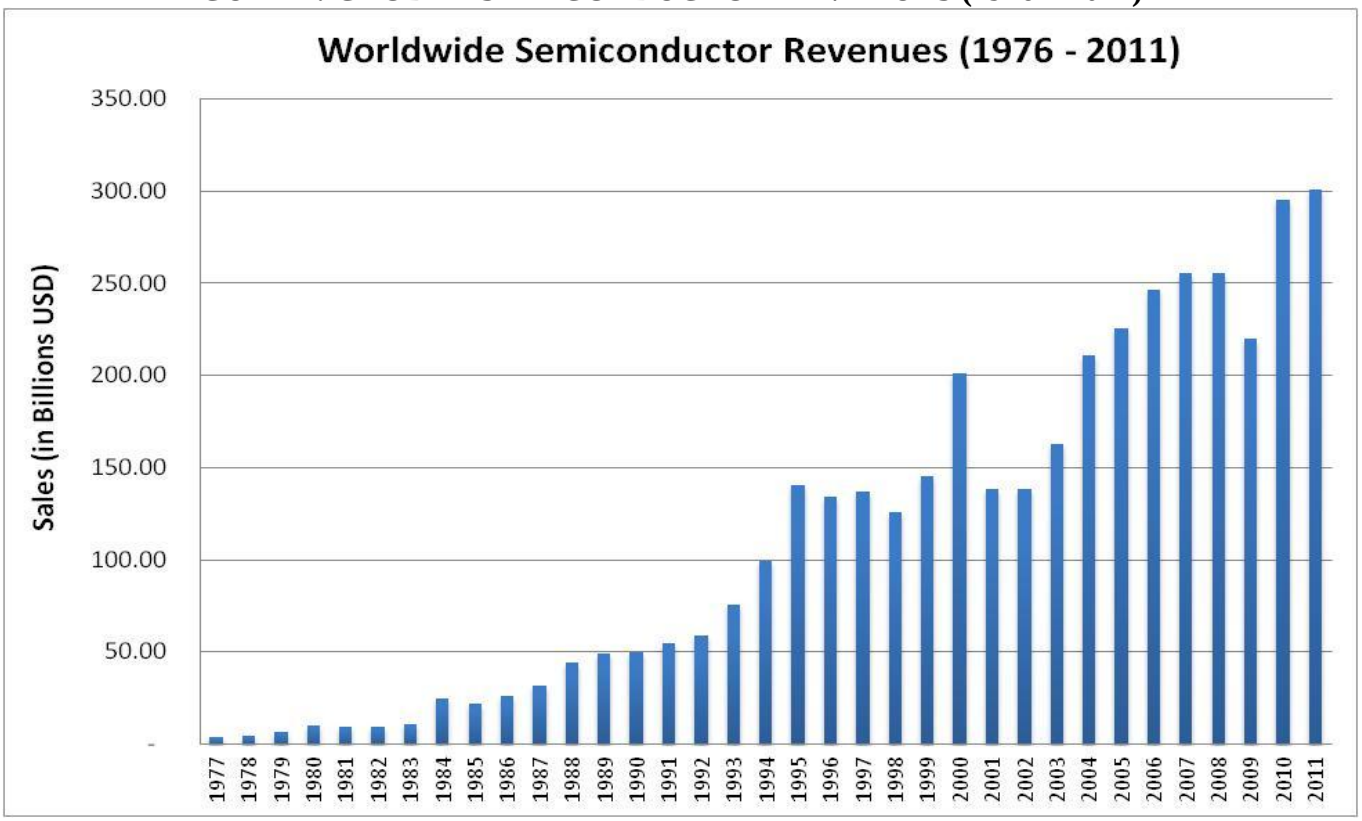
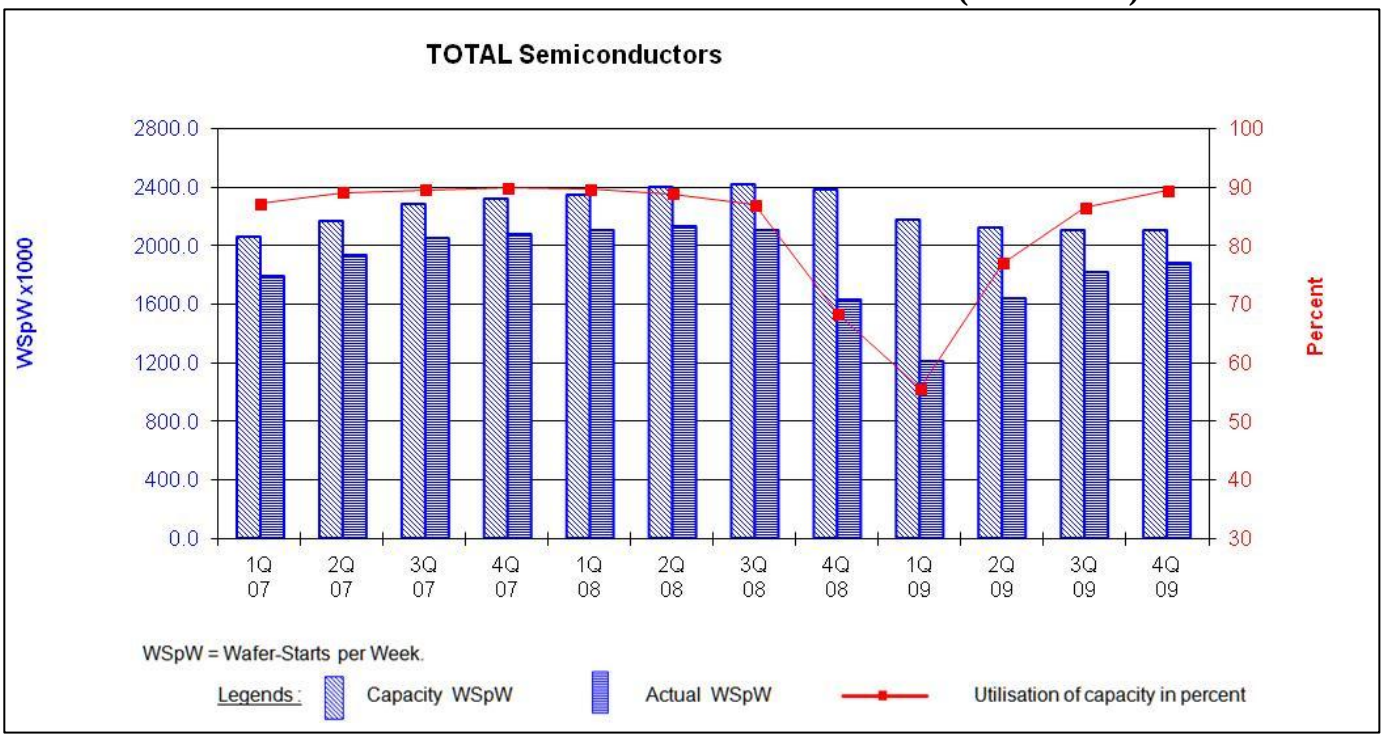


FIGURE 2: TOTAL SEMICONDUCTORS CAPACITY (2007 – 2009)



Source: SICAS Statistics Report, 4Q, 2009

to "connect" with the world almost at all times (Global Semiconductor Market Forecast to 2015, 2012). Because of this huge demand from the market, a huge number of software companies, internet distribution, service providers, and telecommunications companies deemed it essential to invest huge sums of capital to build and expand the infrastructure, which would in turn support the internet and mobile communications (Paccial, 2011). Setting up this infrastructure requires millions and millions of parts (Hong, 2011), which were in turn, produced by the semiconductor industry. Most semiconductor companies enjoyed unprecedented revenues and earnings (Gross & Hester, 2002), since these companies form the backbone of the new economy.

During the boom years, the production capacity of semiconductor companies and their subcontractors are fully utilized. Due to the nature of the production process (Mönch, Fowler, Dauzère-pérès, Mason, & Rose, 2011), the manufacturing schedule follows the plan set according to the orders of the corporate customer. Seldom are special orders given priority. Even if the customer wants some parts delivered faster, the customer cannot do anything but to wait (Groneveld, 2011). It is the sellers, the semiconductor companies, who dictate the terms of delivery. In most cases, delays in delivery cannot be helped because of the very nature of the production process. Due to this foreseen delay in delivery, customers usually order more than what they need so that they would have enough stocks in their inventory (Groneveld, 2011). This practice is usually done so that just in case the customers would have additional orders, they do not have to wait for months before they get their parts.

Sometimes, when the customer badly needs a part and the existing supplier cannot accommodate the order, the customer would tend to look for another vendor who is able to supply the required parts at the fastest possible time. However, transferring to another vendor is not a guarantee of faster and on-time deliveries (Hsu & Sha, 2007), because of the limitations of the production process. Also, if the alternate vendor is already utilizing its full production capacity, it will be very difficult for the vendor to entertain additional orders. This situation is true when business is good, demand is up, and most facilities of semiconductor companies are fully loaded.

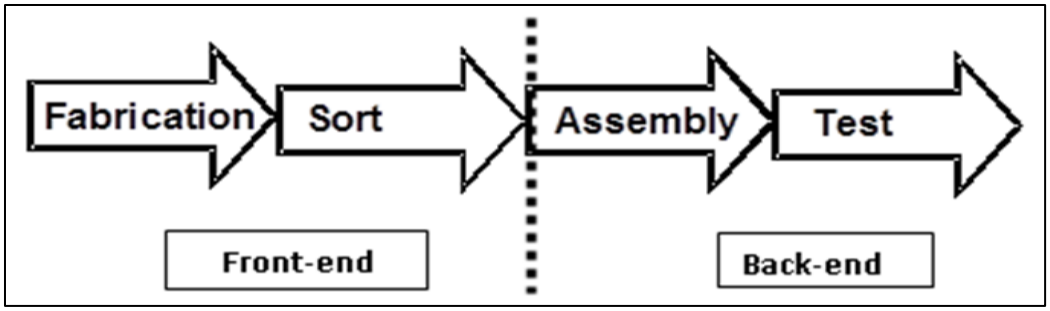
Meanwhile, when bookings are low and business is sluggish, semiconductor companies are very aggressive in scouring for orders. The tables are now turned, the market becoming a buyer's market. Corporate customers now have the luxury to choose which vendor to place their orders from. Companies who are able to deliver their parts the fastest usually gets the most orders. During lean times, corporate customers do not follow the normal procedure of advanced bookings and ordering lead times anymore (Groneveld, 2011). According to Hong and Groneveld, customers rarely order to stock for inventory and order only on "as needed" basis. Thus, one of the keys to surviving during the lean times is to somehow try to shorten the production cycle times and improve the delivery time to the customer (Christie & Wu, 2002).

The main purpose of this paper is to discuss the challenges of managing the semiconductor process to fulfill various product demands from clients. A case study using an actual production process of a particular semiconductor part, the Junction Field Effect Transistors (JFET) is used to illustrate the significance of having an effective yield prediction system in place. JFET products manufactured using a diffusion process to define the channel path has variable process yields, thus it was used as an example in this paper.

II. THE PRODUCTION PROCESS

There are various types of parts being produced by semiconductor companies but most of them follow this standard production process as illustrated in Fig. 3:

FIGURE 3: SEMICONDUCTOR TYPICAL MANUFACTURING PROCESS



The length of the production process varies depending on the type of product, and normally, the bottleneck of the production process is in the fabrication and sort testing of the wafers (Mönch, Fowler, Dauzère-pérès, Mason, & Rose, 2011). This process is normally called in the industry as the "front-end" production process. Some products take as much as twelve (12) weeks before the fabrication process is done. After the fabrication of the wafers, they have to go through wafer sorting before they can be assembled and tested. The products can only be shipped to the customer after it has passed through testing.

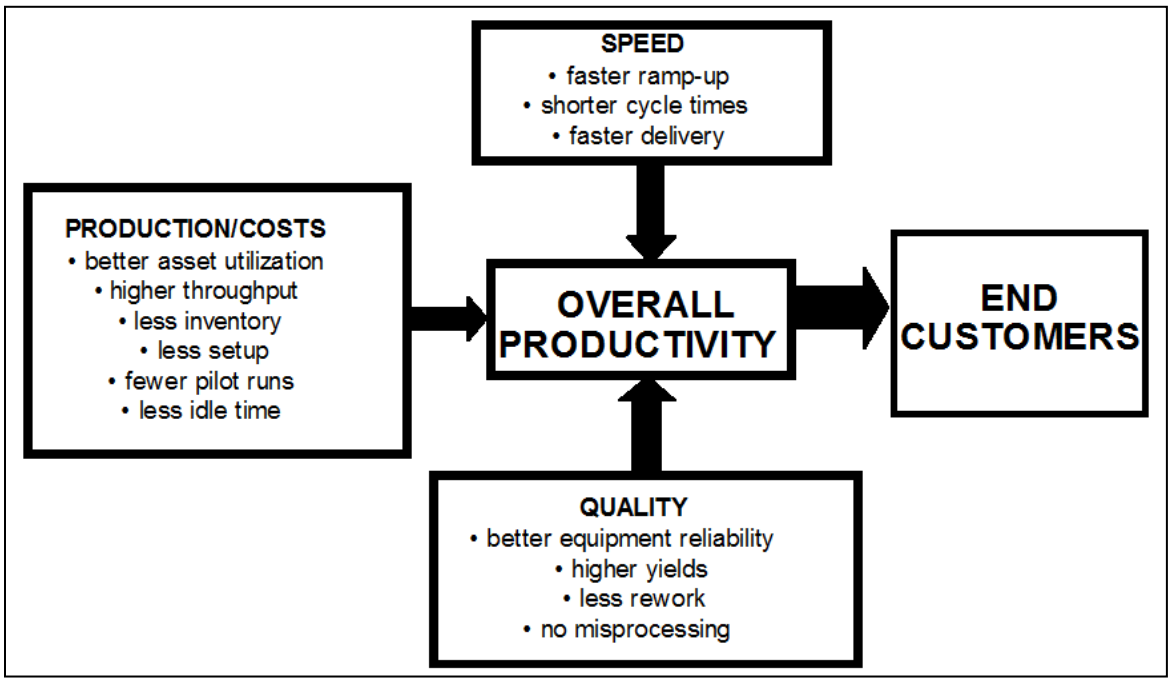
The total cycle time for a typical part, from fabrication to testing, is about two to four months (Hong, 2011). This means that from the time the customer places his order, it would take a little more than three to four months for the semiconductor company to be able to deliver the finished products to the customer. This lengthy production process is the reason why customer bookings and orders have to be made in advance. It is standard industry practice to get customer bookings and orders in about three to six months in advance (Hsu & Sha, 2007). This system ensures that the semiconductor companies have enough time to plan out their production and logistics system. When there is excess capacity, some companies employ parallel loading in their facilities just to be able to shorten the cycle time (Huh, Roundy, & Cakanyidirim, 2006). However, if most of the plant equipment is running at full capacity, outsourcing or capital spending is usually the norm. Any one of these two alternatives would translate to increased material and production costs.

In the semiconductor industry, overall productivity is defined by three major factors: quality, costs of production, and speed, illustrated in Fig. 4. Efficient plant operations will lead to total lower manufacturing costs. Although the costs of quality would entail higher initial capital investment, its long-term effects on cost are well worth it (Bridwell & Richard, 1998). On the marketing side, the faster a company can bring its products to the customers, the higher the satisfaction. Although some customers put a lot of importance on faster delivery, speed to market is not the only consideration. The quality of the product also plays a part. The combination of speed and quality is what counts for the customer.

III. MARKETING AND FINANCE ISSUES

Semiconductor companies mostly sell to the business market, e.g., resellers and distributors (Groneveld, 2011). Parts produced by semiconductor companies are also used primarily as OEM (original equipment manufacturer) parts in consumer goods. When the demand for a certain consumer electronic product is forecasted, the companies that manufacture these consumer products, in turn, will program their orders from semiconductor companies. When the end-consumer demand suddenly shoots up, and the inventories of the companies starts to get depleted, these same companies will now demand "additional"

FIGURE 4: FACTORS AFFECTING PRODUCTIVITY



deliveries from the semiconductor companies. Herein lies the problem.

The lengthy cycle time of the production process limits the ability of the semiconductor companies to react faster to unexpected changes in customer orders (Tierney, et al., 2012). By the time the semiconductor companies are able to deliver, the market demand has already waned. The result is lost revenue opportunity both for the semiconductor and the customer companies.

Sometimes, even if the semiconductor companies are able to deliver the parts, these are rejected because of poor quality. These rejected parts go through failure analysis and if these parts can be reworked, it goes through the production process for the necessary corrections (Sha & Hsu, 2004) so that it can be shipped back to the client. Not only is this system expensive, but it also wastes too much resource. Furthermore, incidents like this tend to make customers very dissatisfied with the company.

IV. PRODUCTION PLANNING PROCESS

Upon receiving the confirmation of orders from the customers, production and business planners use a projected process yield to compute back the number of wafer starts needed to support a certain order quantity. This projected yield helps the production department determine the quantity of wafers that needs to be fabricated to fulfill a specified ordered quantity. These process yields are obtained from the different factory locations around the world that would be involved in the processing of the specific product ordered (Geng, 2009).

Process variations in any part of the production process would alter the projected output and would greatly affect the delivery commitments. To resolve this, process controls are put in place to detect any shift in the process parameters. Additional yield guard bands are also added in yield forecasting to buffer additional loss due to unforeseen and unexpected process variability.

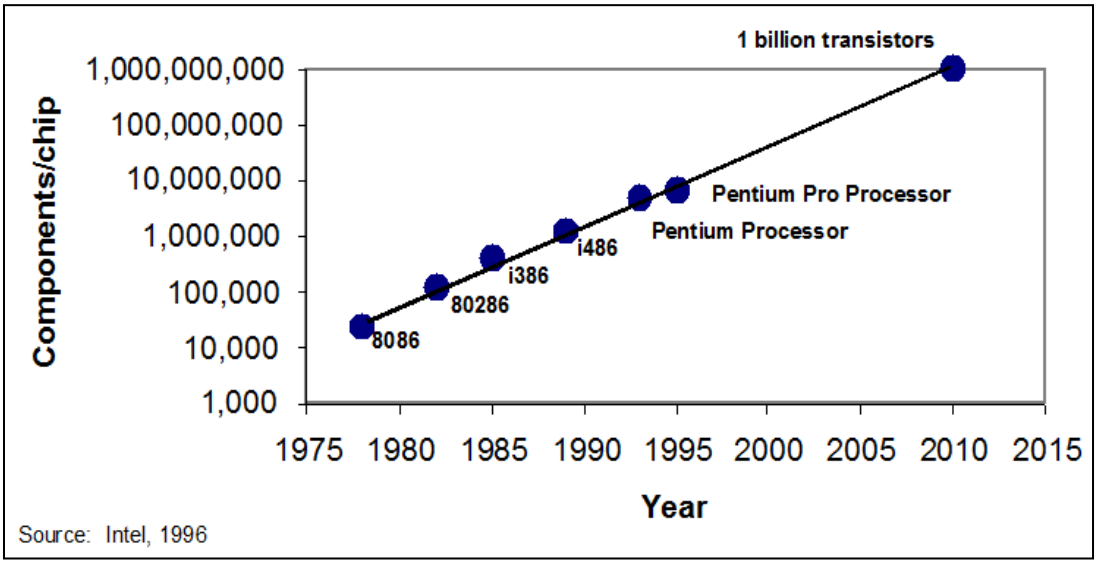
New IC (Integrated Circuit) devices are becoming more complex as technology advances through the years. The cell geometry shrinks at a rate matching Moore's Law, as shown in Fig. 5, wherein the number of transistors that can be

integrated into a given area would double every 18 months.

The complexities of these new IC's result to new and more subtle failure mechanisms that are currently being identified. Existing test equipment has to be updated to keep up with the new generation of IC's that are being produced. It is becoming more and more difficult to detect product failures at an early stage. More often than not, before a device failure is detected, the product has already reached its few final stages. The fabrication processes of these sub-micron level geometry devices require more stringent controls to ensure the quality of the products that come out.

The existing method currently being used in the industry is to sample test some wafers at the wafer sorting facility and to identify the types of devices that can be built from it. This method provides a sort of checkpoint to determine if the wafers can still support the forecasted ordered quantity for the device. If not, then additional wafer loading will have to be started at this early stage.

FIGURE 5: MOORE'S LAW



V. THE IMPORTANCE OF YIELD PREDICTION: A CASE STUDY

Some product types already have defined yield prediction procedures (Chung & Huang, 2002). This makes the backend process for these products a little easier. Yield production for these products follow a standard set of procedures, which would reliably predict the yield based on identified key parameters. However, there are still a number of other devices that require more intricate methods of yield prediction. This is due to the interaction between the different process and device parameters. The very nature of these products makes yield prediction much more difficult and complicated. Although quantitative in nature, the yield prediction methods most often used for these types of products rely mostly on the experiences of the people analyzing the data (Garcia, 2011).

To address customer delivery and quality concerns, it is an accepted industry practice to over-stock on wafers and over-produce the required parts (Hong, 2011) (Garcia, 2011). This practice enables semiconductor companies to ship their parts faster whenever a corporate customer decides to order extra units. If the delivered devices fail, then there will always be more finished good units left in inventory ready for shipment. This practice of overstocking wafers is a good strategy for the sales thrusts of the company, because products can be readily

delivered in cases where the yield prediction is inaccurate. However, this practice puts a huge strain on both the financial resources and production capacity of the company (Scott & Pisa, 1997), especially if the stocked parts are not ordered or sold by year-end. Unsold products are usually scrapped after being kept for a defined period of time.

Unreliable methods of identifying wafers often result to extra long throughput times in processing the semiconductor devices. Companies also tend to incur huge inventories for assembled and tested devices that have no orders. Million dollars worth of this binned inventory are scrapped annually. This is an area where good yield prediction is needed.

To highlight the importance of yield prediction, an illustration of a specific product and its yield is used. Table 1 shows an actual yield example for the Junction Field Effect Transistor (JFET) product, wherein lot number BBN35C8 was erroneously predicted to have a 25% sub-product or binsplit yield using wafer level process/device parameter data. However, after the wafer lot went through the production process, the actual sub-product yield that came out was only 1.95%.

TABLE 1: JFET BINSPLIT PERFORMANCE

Lot#	Lot Size	Test Yield	Estimated binsplit	Actual Binsplit
BBN35C8	28645	>97%	25%	1.95%
BBP01C2	29655	>97%	17%	0.78%
BBP01C3	20043	>97%	15%	0.26%

Table 2 presents an example of a customer order and quantity requirement. It shows how an erroneous yield projection results to a huge production problem. For instance, if a customer ordered 100,000 units of product X, with a binsplit yield prediction of 25%, the wafer start quantity required would be 600,000 units. With the new actual yield of 1.95%, the required wafer start quantity now shoots up to 7.4 million units. Immediately, there is a difference of 6.8 million units for wafer starts. The initial wafer start of 600,000 units produced only a measly 8,190 good units. An additional 6.8 million units would have to be produced by the fabrication plant to be able to fulfill the customer order of 100,000 units.

TABLE 2: WAFER START QUANTITY FOR PRODUCT X

Ordered Quantity	Binsplit assumption	Required wafer start quantity
100,000 units	25.00%	600,000 units
100,000 units	1.95%	7,400,000 units

This error in yield prediction means that the fabrication plant has to produce more wafers to fulfill the unsupported order requirements of the customer. With a gestation period of about 8 to 12 weeks, by the time the final product comes out of the factory, the customer might not require it anymore, or worse, could have ordered the parts from a competitor.

The impact on operations is much worse. This development is similar to pressing the panic button on the production floor. The pressure is for the fabrication plant to come up with the required number of wafers as soon as possible to salvage the situation. All existing products already in process would be de-prioritized to fast track the new wafer lot across the production process. This will cause undue stress on the whole production system and delays in the deliveries of products that were temporarily taken off the production floor.

There have been many types of analysis tools developed to correlate fabrication / wafer level data to the device-level performance. However, majority of the existing yield prediction tools used on wafer level data focus mainly on statistical analyses based on minima/maxima values, the standard deviation, and percentile distribution of the parameters. There have been few studies made on the parameter interaction of these test data. Interactions between the different process parameters and the difficulty in getting a direct correlation between them have made this difficult. Very few known methods include parameter interactions in their analyses. These parameter interactions, together with the other statistical data would greatly affect the eventual yield of the device.

5.1 The Monte Carlo Simulation Method as Applied to Yield Prediction

There are different yield simulation tools available. For this study, the Monte Carlo simulation approach as applied to yield prediction is used. Wafer level data are used in these simulations to predict the resulting device performance at the back-end final test. This tool can also be used by both engineering and planning groups in their yield and production capacity planning and analysis.

Monte Carlo is a statistical simulation based on numerical method that allows the drawing of a value of a random variable X from a population with known probability density distribution, p(x) in the interval [a,b] (Co, Lim, & Caluyo, 2001). The values of Y can be generated by the use of pseudo-random number generators and is distributed in the interval [0,1]. Equation (1) below shows the relationship between X and Y:

$$Y = \int_{a}^{X} p(x)\, dx \qquad (1)$$

For the Monte Carlo method to apply, each variable or parameter to be studied should have a probability density function. Since the probability density function p(x) of the population are not generally known, the probability density function of the population can be approximated by calculating the probability density function of the samples. These probability density functions depend on the process and therefore vary from device to device and from one parameter to another.

In order to do the simulations, there should be a way by which a value of X can be obtained for each corresponding value of Y. Since it is not possible to directly solve for X for each value of Y from equation (1), the cumulative probability distribution is generated from the probability density function indirectly graphically. Obtaining the value of X for each value of Y becomes a matter of table look-up combined with an interpolation technique or using a simulation tool. The drawing of these values of X, can be simulated as many number of times as one wishes. In general, as the number of simulations increases, the distribution of X approaches the actual p(x).

5.2 Calculating the Yield of a JFET transistor using Simulation

Table 3 shows an example of an actual JFET transistor datasheet parameters.

TABLE 3: JFET TRANSISTOR PARAMETERS

	Vth	BVgs	Ig-lkg	Id-lkg	Rds
	Volt	Volts	PicoAmp	MilliAmp	Ohm
Min	2.1	41	0	0	26.3
Max	4.9	100	80	57	71.2

Table 4 shows the e-test (electrical test) parameter distribution for a given JFET transistor wafer lot. This given lot yielded 48.48% in actual production for the specified parameter value in Table 3.

TABLE 4: TRANSISTOR E-TEST DATA

	Min	10%ile	50%ile	90%ile	Max
Vth	1.05	2.14	2.63	2.99	3.23
BVgs	23	43.9	51.8	54.6	55.5
Ig lkg	27	29	34	54	81
Id lkg	1.7	17.8	26.9	64.7	125
Rds	8	43	50	68	129

Yield is equal to the ratio of the number of good working devices to the number of devices obtained from a production lot. The yield of a device depends upon a certain number of parameters, all of which must be within acceptable limits for the device to function properly. For a device to be considered good, all of the parameters should be within the minimum and maximum acceptable limits.

Each simulation involves the generation of random values of the five parameters that affect the yield of the transistor device. This is done by generating 5 random numbers uniformly distributed between 0 and 1. Each of these numbers represents the random variable Y, which is used to generate the corresponding values of the five parameters. If all of the 5 parameters are within acceptable limits, the device is considered to be acceptable. Otherwise, the device is considered non-working. The simulation is repeated N number of times. Yield is calculated as the ratio of the total number of acceptable devices to the total number of simulations, N. A MATLAB program was used for the simulations.

Fig. 6 and Fig. 7 show two examples of the relative frequency distributions from Parameter 1 and Parameter 2. The line represents the actual values while the circles represent points that were generated using simulation. It can be seen in Fig. 6 and Fig. 7 that the distribution of the simulated points, represented by the circles, closely resembles the actual frequency distributions of the raw data, represented by the line curve.

Fig. 8 and Fig. 9 show the corresponding cumulative probability distributions of the two based on sampled data values. The cumulative distribution curves are used to calculate values of each parameter, represented by the random variable, X, from corresponding values of random variable Y uniformly distributed between the interval [0,1].

Table 5 shows the comparison between the mean and standard deviations of the actual and simulated values of the transistor parameters. It can be seen that for most of the parameters, the simulated and actual data are quite close to each other. Any big discrepancy between actual and simulated results can be explained by the fact that the raw data that were collected for the transistor have quite a number of data values that are either too big or too small which have drastically changed the statistics of the data.

Nevertheless, one simulation involving N=1000 gave a predicted yield of 46.76% as compared with the actual yield of 48.48%. These results show that there is good agreement between the predicted and the actual yields.

Sensitivity of the results to the number of simulations—Table 6 shows the values of the yield for different number of simulations, N. It can be seen that the simulated values of yield compare favorably with the actual value, which is 48.48%. It can be noted likewise that the predicted value of the yield does not vary much with the number of simulations used. Any small

FIGURE 6: RELATIVE FREQUENCY DISTRIBUTION OF PARAMETER 1

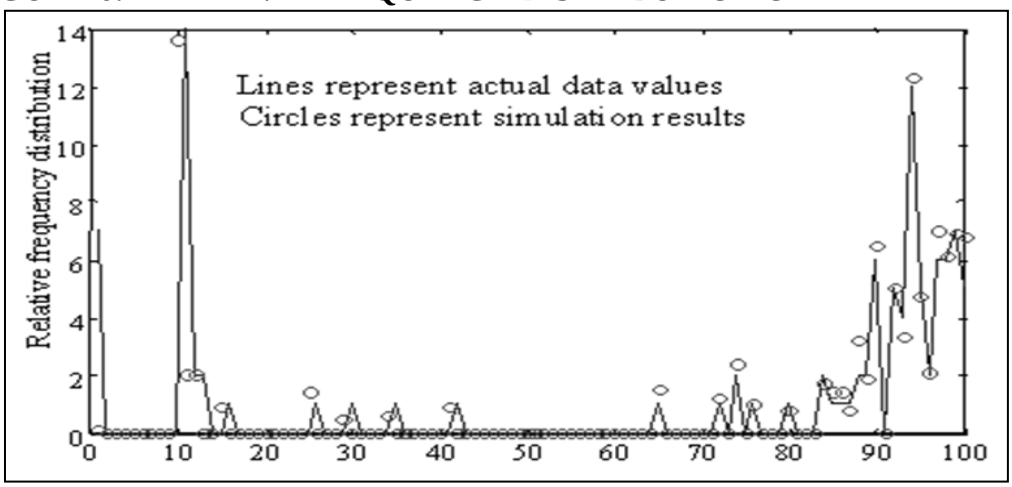


FIGURE 7: RELATIVE FREQUENCY DISTRIBUTION OF PARAMETER 2

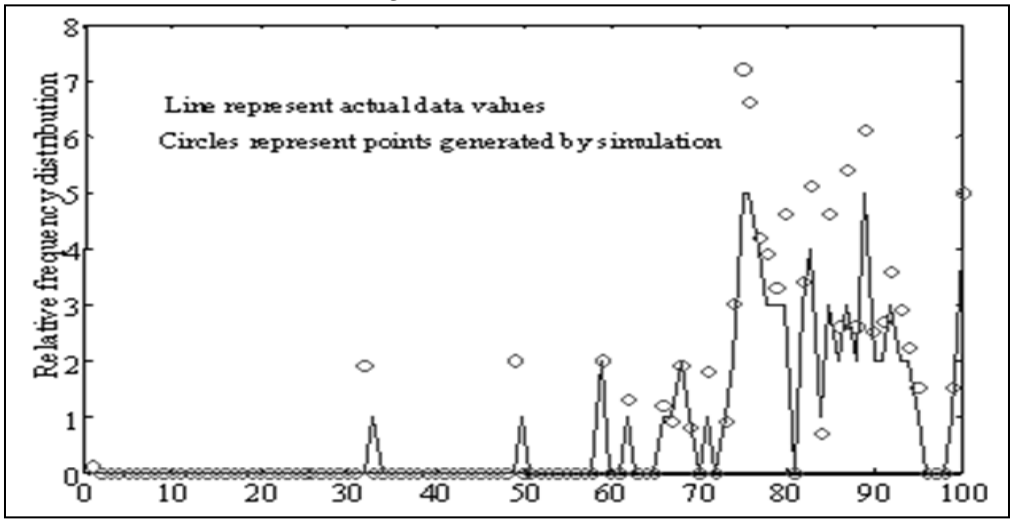


FIGURE 8: CUMULATIVE PROBABILITY DISTRIBUTION OF PARAMETER 1

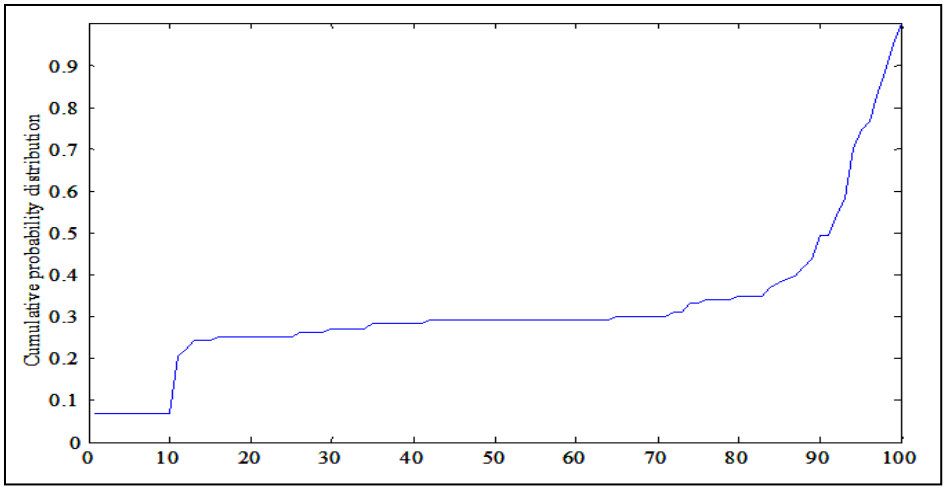


FIGURE 9: CUMULATIVE PROBABILITY DISTRIBUTION OF PARAMETER 2

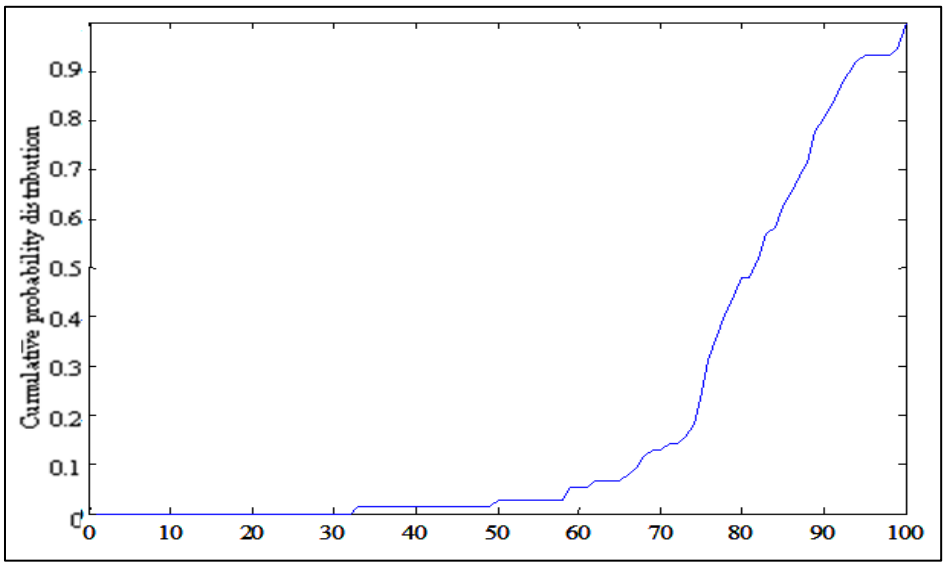


TABLE 5: COMPARISON OF THE MEAN AND STANDARD DEVIATION BETWEEN ACTUAL AND SIMULATED VALUES OF THE TRANSISTOR DEVICE

Average Values					
	Vth	BVgs	Ig-Lkg	Id-Lkg	Rds
Actual	1.69	38.07	33.08	20.40	19.42
Simulated	2.53	40.26	34.02	14.90	21.56
Standard Deviation					
	Vth	BVgs	Ig-Lkg	Id-Lkg	Rds
Actual	1.61	20.87	6.13	98.60	13.87
Simulated	0.39	18.64	6.01	88.80	14.38

discrepancy can be attributed to inherent simulation error particularly in the generation of pseudo-random numbers. This also suggests that some degree of pre-processing of raw data may be needed to obtain probability density functions that reflect the actual statistics of the population.

TABLE 6: YIELD AS A FUNCTION OF THE NUMBER OF SIMULATIONS

Number of Simulations	Yield (%)
500	44.01
600	43.943
700	44.482
800	43.162
900	45.509
1000	46.76

VI. CONCLUSION

Accurate and proper yield prediction can help the management plan their operations activities more effectively. Although, there have been different methods used in predicting device yield performance, the best method is to consider

wafer level parameter interactions in the analysis of device yield performance. The Monte Carlo Simulation can be used as a good yield prediction as illustrated in the case study.

The plant capacities of each company-owned factory and subcontractor facility could be more efficiently allocated. Each site can run their own production smoothly, with minimal problems on setup time and costs. Production capacity is efficiently utilized when production schedules are on-track. Similarly, the fabrication processes are not disrupted because of additional wafers that need to be rushed through production in cases when the variances between the actual and predicted yields are significant.

In the same manner, the jobs of the people in marketing, sales and customer service departments are made a lot easier. They would be able to fulfill commitments to client companies. The specified quantity of the products will surely be delivered on the agreed schedule between the company and the customer. Losing customers due to failures in delivery commitments will be minimized. In the cutthroat semiconductor industry, customer retention, product quality and on time delivery are critical priorities. If these priorities are being met by predictable and reliable product outputs, company resources can be re-focused on market expansion and new product development.

All these developments translate to a reduction of overall production and product costs. Good yield prediction creates a domino effect. On the operations side, production can run smoothly and according to planned schedules all throughout the year. There is minimal idle time due to lesser down time in equipment and human resource. Scraps on the production floor will be minimized with more products going to the customers rather than stay in warehouses as binned inventory. Asset utilization would be maximized. Asset turnaround time and inventory turnover would be shorter, resulting to a more efficient use of capital. The result is increased productivity and efficiency for the company as a whole.

Further study can be done using different yield prediction tools as applied to different types of semiconductor products. The choice of the yield simulation model to use should take into consideration the different process parameters of the individual products.

REFERENCES

(2002). 2001 *Billings Figure Reflects 41% Year-over-Year Decline*. Santa Clara: SEMI.

Bridwell, L., & Richard, M. (1998). The Semiconductor Industry in the 21st Century: A Global Analysis Using Michael Porter's Industry Related Clusters. *Competitiveness Review*, 24-36

Caroline Kamierski. (2012). *Semiconductor Industry Posts Record-Breaking Revenues Despite 2011 Challenges*. Santa Clara: SIA.

Caroline Kazmierski. (2012, May 15). *Semiconductor Industry Association*. Retrieved May 16, 2012, from Semiconductor Industry Association: http://www.sia-online.org

Chen-Fu, C., & Chien-Hung, C. (2007, October). *A Novel Timeteabling Algorithm for a Furnace Process for Semiconductor Fabrication with Constrained Waiting and Frequency-Based Setups. OR Spectrum* , pp. 391-419.

Christie, R. M., & Wu, S. D. (2002). Semiconductor Capacity Planning: Stochastic and Computational Studies. IIE Transactions , 131-143.

Chung, S.-H., & Huang, H.-W. (2002). Cycle Time Estimation for Wafer Fab with Engineering Lots. *IIE Transactions* , 105-118.

Co, C., Lim, F., & Caluyo, F. (2001). JFET Yield Prediction Using Monte Carlo Simulation Method. *ASEAN Science and Technology Conference* (pp. 191-209). Brunei: ASEAN Microelectronics and Technology.

Garcia, R. (2011, March 4). Product and Process Manager. (F. Lim, Interviewer)

Geng, G. (2009). Stochastic Programming Based Capacity Planning for Semiconductor Wafer Fab with Uncertain Demand Capacity. *European Journal of Operational Research* , 899-908.

(2010). *Global Chip Sales Decline in 2009*. San Jose: SIA.

(2012). *Global Semiconductor Market Forecast to 2015*. New York: PR Newswire.

(2001). *Global Semiconductor Market to Rebound in 2002*. Washington: Semiconductor Industry Aassociation.

Groneveld, P. (2011, January 27). Director of Product Marketing. (F. Lim, Interviewer)

Gross, A. C., & Hester, E. D. (2002, July). The Global Electronic Components Industry. *Business Economics* , pp. 59-65.

Hong, L. (2011, February 9). General Manager. (F. Lim, Interviewer)

Hsu, S., & Sha, D. (2007). The Integration of Shop Floor Control in Wafer Fabrication. *Journal of Manufacturing Technology Management* , 598-620.

Huh, W. T., Roundy, R. O., & Cakanyidirim, M. (2006). A General Strategic Capacity Planning Model Under Demand Uncertainty. *Naval Research Logistics* , 137-150.

Lara Chamness. (2012). *Worldwide Semiconductor Market Historical Report* (1991-2011). Santa Clara: SEMI.

Lara Chamness. (2012). *Worldwide Semiconductor Market Statistical Historical Report* (1991-20110. Santa Clara: SEMI.

Lim, F., Caluyo, F., & Co, C. (2002). Device Performance Prediction Using Monte Carlo Simukatoni Method. *SEMI Technical Symposium* (pp. 58-72). Manila: SEMI.

Macher, J. (2006). Technological Development and the Boundaries of the Firm: A Knowledge-Based Examination in Semiconductor Manufacturing. *Management Science* , 583-599.

Makani, B., Lim, F., Caluyo, F., & Co, C. (2003). A Heuristic Approach to Process and Enterprise Modeling and Simulation Based on the Monte Carlo Method. *International Conference on Production and Research* (pp. 18-32). Blacksburg: Academy of Production and Research.

Mönch, L., Fowler, J. W., Dauzère-pérès, S., Mason, S. J., & Rose, O. (2011). A Survey of Problems, Solution Techniques, and Future Challenges in Scheduling Semiconductor Manufacturing Operations. *Journal of Scheduling* , 583-599.

Moore's Law Extended: The Return of Cleverness. (2007, July). *Solid State Technology* , pp. 28-36.

Paccial, D. (2011, January 21). Capital Controller. (F. Lim, Interviewer)

Scott, D., & Pisa, R. (1997). Can Overall Factory *Effectiveness Prolong Moore's Law?* Santa Clara:\ Solid Sate Technology.

Sha, D., & Hsu, S.-Y. (2004). The Effects of Rework on the Shopfloor Control in Wafer Fabrication. \ *Journal of Manufacturing Technology Management* , 184-198.

(2010). SICAS *Annual Capacity Report*. Netherlands: SICAS

Sobol, I. (1975). *The Monte Carlo Method.* Moscow: Mir Publishers.

Tierney, R., Groen, A. J., Harms, R., Luizink, M., Hetherington, D., Stewart, H., et al. (2012). Managing Highly Flexible Facilities: An Essentail Complementary Asset at Risk. *International Journal of Entrepreneurial Behaviour & Research* , 233-255.

Walpole, R. E., & Myers, R. H. (1996). *Probability and Statistics for Engineers and Scientists.* New York: MacMillan.

Wu, S. D., Erkoc, M., & Karabuk, S. (2005). Managing Capacity in the High-Tech

Industry: A Review of literature. *The Engineering Economist* , 125-158.